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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,720	12/16/2003	Tokio Miyasita	030712-20	3461

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EXAMINER	
JACKSON, BLANE J	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,720	MIYASITA ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with regard to new claims 34 and 35 filed 13 December 2006 have been fully considered but they are not persuasive. The applicant asserts, in view of new claim 34, the combination of prior art references fail to disclose gate resistances, which are respectively connected to the gate of the third and fourth transistors. However, secondary reference Shkap teaches a variable gain RF amplifier utilizing three transistors coupled in series between the emitter legs of a differential transistor pair to degeneratively control the gain of the amplifier. This gain control circuit comprising three transistors also includes two resistors, figure 1, resistors (11) and (12), that are coupled to the gain control voltage and individually connected to the gate of two of the three transistors to effect impedance or bias control of the transistors. Even though Shkap teaches a gain control circuit that is larger in scope than is claimed, the circuit of Shkap is considered to read on this particular claim element.

Specification

The amended Title filed 13 December 2006 is accepted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shkap (US 6,414,547) in view of Si (US 6,894,563).

As to claim 34, Shkap teaches a variable gain amplifier comprising:

a differential input amplifier which includes transistors T1 and T2 that constitutes a differential pair (figure 1, column 1, line 66 to column 2, line 4, emitter-cou0pled pair of bipolar transistors 1 and 2 used as a gain stage),

a variable impedance connected between the *emitters* of the respective transistors T1 and T2 of said differential input amplifier (column 2, lines 22-34, gain control device comprised of transistors (3, 4 and 5) connected in series between the emitter leads of transistors 1 and 2 subject to a control voltage to control the presented variable resistance which effectively degenerates the transconductance of the input differential transistor pair),

a constant current circuit that operates as an absorption current circuit for the transistors T1 and T2 constituting the differential pair wherein the constant current circuit includes a first constant current circuit and a second constant current circuit (column 2, lines 13-21, inductors (13 and 14) present a high impedance path at the RF operating frequency and provide a DC short circuit to ground potential terminal (21) with

respect to a bias voltage applied through conventional biasing means to the base of transistor pair 1 and 2),,

said first and second transistors constituting said differential pair have their gates respectively connected to first and second differential inputs, have their drains respectively connected to ends of first and second load resistances being respectively connected to a supply voltage at their other end and have their source respectively connected to the first and second constant current circuits (figure 1, column 2, lines 1-12, load resistances in this amplifier comprising the primary of transformer (15), which is an inductive impedance to the operating RF frequency, with a center tap to a DC voltage source),

third and forth transistors with drain-source paths of the third and fourth transistors which serve as said variable impedance are connected with the source of said respective first and second transistors (figure 1, the gain control device including NMOS transistors (3, 4 and 5)), and

a gain control voltage is connected to gates of the third and fourth transistors via first and second gate resistances respectively whereby a gain of said differential input amplifier is variably controlled by controlling a value of said variable impedance (figure 1, column 2, lines 31-53, the gates of NMOS transistors (3 and 5) receive a gate voltage via resistors (11 and 12) respectively, transistor (4) directly, to control their respective impedance for emitter degeneration).

Shkap teaches a gain control device including three NMOS transistors coupled between the emitters of the respective input differential pair of bipolar transistors 1 and

2, column 2, lines 22-30, to function as a voltage controlled variable resistance for gain control, but does not teach the variable impedance is connected between the *sources* of the respective transistors where "sources" indicates transistors 1 and 2 are field effect type transistors (FET).

Si teaches automatic gain control of a differential amplifier also using variable degeneration resistance, figure 2. Si discloses the variable resistance of degeneration transistors (M8) and (M9) are field effect transistors connected between the current source (M5) or ((M10) and the respective amplifier pair FET transistors (M6) and (M7), column 3, lines 38 to column 4, line 10.

Since Si teaches the automatic variable resistance degeneration circuit may be applied to a voltage to current (bipolar transistor) input differential pair or a voltage to voltage (FET) input differential pair, column 1, line 66 to column 2, line 39, it would have been obvious to one of ordinary skill in the art at the time of the invention to realize the bipolar transistors and associated biasing in the input differential amplifier pair of Shkap may be exchanged for a field effect transistor pair as taught by Si to have voltage to voltage rather than a transconductance type gain topology.

As to claim 35, Shkap teaches a variable gain amplifier according to claim 34 further comprising a gain control device including capacitor (9), resistor (11), resistor (11) and capacitor (10) coupled in parallel with the series coupled variable impedance transistors (3, 4 and 5) that functionally provide biasing to the variable impedance transistors as well as a resistance at the RF operating frequency which would determine

a minimum gain of the differential input amplifier, and which is connected between said sources of the first and second transistors, column 2, lines 31-53.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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